

PowerPC 440EPx

Embedded Processor



With speeds of up to 667 MHz, support for floating-point operations, USB 2.0, Gigabit Ethernet, security and NAND Flash interfaces, low power dissipation and a small footprint, the PowerPC 440EPx embedded processor is ideally suited to a wide range of high-performance applications, including imaging, industrial control and networking.

Benefits

- Delivers 400 MHz to 667 MHz performance (CPU)
- DDR1/2-333 memory support
- Single/double-precision floating point unit for math-intensive applications
- 10/100/1000-Mbit/s Ethernet support
- Security (optional)
- On-chip memory
- NAND Flash support
- Extensive connectivity by means of on-chip Ethernet, USB, UARTs, IIC, SPI and PCI
- Offers low power dissipation and small form factor for high-density and power-conscious applications

The PowerPC 440 Core

To enhance overall throughput, the PowerPC 440 superscalar core incorporates a 7-stage pipeline and executes up to two instructions per cycle. Its large 32-Kbyte data cache and 32-Kbyte instruction cache are 64-way set-associative. Versatile configurations enhance performance tuning while optional parity protection preserves data integrity. For additional system performance, the PowerPC 440 core includes dynamic branch prediction and 24 multiply accumulate instructions (MAC) that can be used for signal processing or other numerical tasks, as well as non-blocking caches that can be managed in either write-through or write-back mode.

High Performance FPU

In addition to its powerful 440 core, the PowerPC 440EPx includes a high-performance FPU. This superscalar FPU supports both single and double precision operations, and offers single cycle throughput on most instructions. The result is exceptional performance in imaging and other calculation intensive applications.

Security (Optional)

On-chip IPsec/SSL Security acceleration engine supporting DES, 3DES, AES, ARC-4 encryption, MD-5, SHA-1 hashing, HMAC encrypt-hash and hash-decrypt and Kasumi. Also supports public key acceleration for RSA, DSA and Diffie-Hellman, and an on-chip true random number generator.

devices are served by two 32-bit on-chip peripheral buses (OPB).

Extensive Memory Support

An on-chip double data rate 1/2 (DDR1/2) SDRAM controller provides a 32/64-bit memory interface with optional error checking and correcting (ECC) and a 2.6-Gbyte/s peak data rate. It supports two memory banks of up to 1 Gbyte each, for a maximum capacity of 2 Gbytes. An integrated NAND Flash controller allows up to four banks of Flash memory devices to be connected to the processor's external peripheral bus. The Flash controller supports device densities up to 512 Mbytes, an optional SmartMedia card interface. These devices can be accessed much like diskette drives, with available boot capability.

On-Chip Memory

The PowerPC 440EPx offers 16 Kbytes of on-chip memory.

PCI Interface

The PowerPC 440EPx offers a 32-bit PCI V2.2 interface and supports frequencies of up to 66 MHz. Multiple read prefetch and write post buffers enhance throughput, while the ability to boot the processor from PCI bus memory increases functionality.

Dual Ethernet Ports

For extensive connectivity options, the 440EPx offers two integrated 10/100/1000 Ethernet ports with Jumbo Frame support. Supports GMII/MII, TBI, RTBI, RGMII, and SMII interfaces.

USB Interface

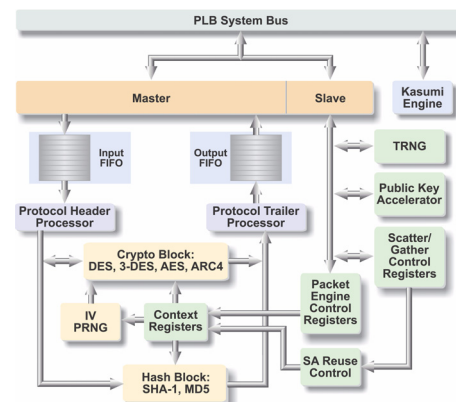
The 440EPx includes USB 2.0 host and device controllers and a single on-chip USB 2.0 PHY on chip. A second USB 2.0 PHY can be attached externally by means of a UTMI interface.

External Bus Interface

To accommodate connectivity with other devices, the PowerPC 440EPx offers a 32-bit bus supporting up to six ROM, RAM or slave peripheral I/O devices and speeds up to 83 MHz. 4-Channel DMA and external bus mastering and also supported.

Standard Peripherals

The PowerPC 440EPx offers support for up to 64 general-purpose I/O (GPIO) and two IIC controllers. A serial peripheral interface (SPI), also referred to as a serial communications port (SCP), allows full-duplex, synchronous data exchanges with other serial devices. The 440EPx also supports up to four UARTs in a variety of configurations. A JTAG interface is provided for debugging purposes.



IPsec/SSL Security Acceleration Engine Block Diagram

High-Speed Bus Architecture

Offering a peak bandwidth of 5.3 Gbytes/s and separate read and write data buses – the PowerPC 440EPx's processor local bus (PLB) provides a high-bandwidth connection between the processor core and memory controller. Less demanding I/O

PowerPC 440EPx

PowerPC Partners Ecosystem

AMCC's embedded PowerPC processors are supported by an extensive ecosystem of products and services from a wide range of leading suppliers. AMCC's PowerPC Partners program includes industry-standard providers of:

- Embedded operating systems
- Hardware and software development tools
- Embedded software products and services
- Board-level products
- System design services
- Technical training.

For full details of the products and services available through the PowerPC Partners program, or to browse support available for a specific processor, visit:

<http://www.amcc.com/Embedded/Partners>

AMCC also provides an evaluation kit for this PowerPC processor, including an optimized evaluation board as well as sample applications and other software.

Features

- Speed (frequency): 400 MHz to 667 MHz
- Performance: 2.0 DMIPS/MHz (1,334 DMIPS @ 667 MHz peak)
- 5-stage FPU with 2.0 MFLOPS/MHz (SP/DP); hardware support for IEEE 754; single-precision and double-precision operation with 32 64-bit floating-point registers
- On-chip IPsec/SSL acceleration (optional)
- NAND Flash controller. Supports one to four banks of NAND Flash memory devices; direct interfacing to discrete NAND Flash devices (up to four devices) and SmartMedia Card socket (22-pins); 4-Mbyte - 256-Mbyte devices sizes supported; 512-byte +16-byte or 2-Kbyte +64-byte device page sizes supported; DMA support allows direct, no processor-intervention block copy from NAND Flash out to SDRAM; boot-from-NAND supported
- On-chip double data rate 1/2 (DDR1/2) SDRAM controller with 32/64-bit interface, 2.6-Gbyte/s peak data rate and optional ECC
- Support for two banks of DDR SDRAM memory of up to 1 Gbyte each, maximum capacity of 2 Gbytes
- Support for 256, 512-Mbit and 1-Gbyte DDR devices, with CAS latencies of 2 or 3
- 32-bit PCI V2.2, 3.3-V interface supporting frequencies of up to 66 MHz
- USB 2.0 device controller, USB 2.0 Host controller and one on-chip USB 2.0 PHY. A second USB PHY can be attached off-chip by means of a UTMII interface.
- (2) Ethernet 10/100/1000-Mbit/s, full-duplex MACs supporting GMII/MII, TBI, RTBI, RGMII, SMII interfaces. Memory access layer (MAL) provides DMA capability to both Ethernet channels
- Up to 83 MHz, 30-bit address bus, 32-bit data bus external bus control (EBC) interface
- Support for up to 6 ROM, RAM, or slave peripheral I/O devices
- 4-channel DMA support for external peripherals
- External bus master controller for access to internal peripherals
- Support for memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers
- Scatter/gather capability
- Up to four UARTs (1x 8-pin, or 2x 4-pin, or 4x 2-pin, or 1x4-pin and 2x 2-pin)
- Two IIC (with one integrated boot strap controller)
- One SPI serial interface
- 4-channel DMA – available for internal and external use

- Programmable interrupt controller with 10 external inputs, 54 internal inputs
- Programmable timers
- General-purpose I/O (64)
- Support for JTAG board testing, JTAG debuggers, and 4xx instruction trace interface
- RoHS compliant version available (lead-free)

For more information, please visit <http://www.amcc.com>.

Specifications

Technology

- 0.13 μ m CMOS

Performance (estimated)

- 800 Dhrystone 2.1 MIPS @ 400 MHz
- 1,334 Dhrystone 2.1 MIPS @ 667 MHz

Frequency

- CPU: 400 MHz to 667 MHz
- Memory: 32/64-bit width: 1.6 Gbytes/s (DDR1/2-200) to 2.6 Gbytes/s (DDR1/2-333)
- PCI: 32-bit, 33 MHz to 66 MHz

Typical Power Dissipation

- <4 W @ 533 MHz (estimated)
- Core/FPU <1.5 W @ 533 MHz

Case Temperature Range

- -40 ° to +85 ° C

Power Supply

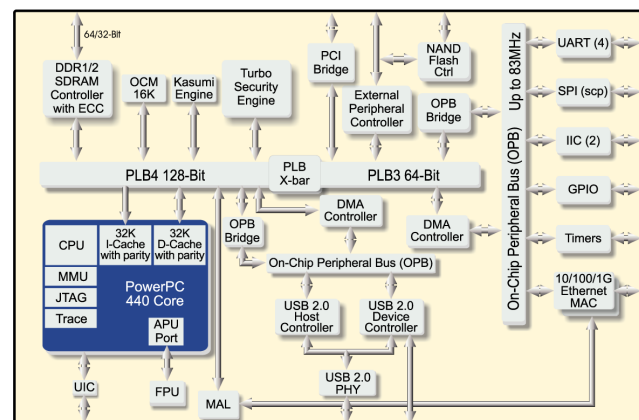
- 1.5 V (logic), 1.8 V (DDR2), 2.5 V (DDR1, Ethernet), 3.3 V (PCI, other I/O)

Signal I/Os

- 367

Packaging

- 680-TEPBGA, 35 mm x 35 mm (with 1-mm ball pitch)



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